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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/164,123	09/30/98	MAYER A	GR-97-P-2681

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EXAMINER	
EATON, K	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/04/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/164,123	MAYER, ALBRECHT	
	Examiner	Art Unit	
	Kurt M. Eaton	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 16-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 16-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/26/01 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-4, 7, and 16-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Hatanaka.

In re claim 1, Hatanaka shows in Figures 1A-1B, 2A-2B, 3, 4, and 5A-5I a method for producing an electrical connection between integrated circuits which includes providing a first integrated circuit having a signal terminal (portion of first conductive layer 6 between I/O pad portion 10 and fuse portion 11) and a terminal (3); forming an electrically conductive connection between the terminal and the signal terminal of the first integrated circuit (11); providing a protective structure (23/24) that becomes conductive to dissipate electrostatic discharges; providing

a second integrated circuit (20) having a terminal that is coupled to the protective structure; disposing the first and second integrated circuits adjacent one another; electrically connecting the signal terminal of the first integrated circuit to the terminal of the second integrated circuit; connecting the terminal of the first integrated circuit to a terminal of a package; and, subsequent to connecting the terminal of the first integrated circuit to the terminal of the package, severing the electrically conductive connection between the terminal and the signal terminal of the first integrated circuit using an energy pulse {column 3, line 5 - column 6, line 11}.

In re claim 2, Hatanaka shows wherein the severing step is performed by applying an electrical current pulse to the terminal of the second integrated circuit {column 3, line 5 - column 6, line 11}.

In re claim 3, Hatanaka shows wherein the forming step includes forming the electrically conductive connection with a portion of reduced cross sectional area as compared to the rest of the connection; and dimensioning the portion to dissipate electrostatic discharges between the terminal and the signal terminal of the first integrated circuit and to be severed during the application of the energy pulse in the severing step {column 3, line 5 - column 6, line 11}.

In re claim 4, Hatanaka shows wherein the energy pulse used in the severing step is an electrical current pulse applied to the terminal of the second integrated circuit {column 3, line 5 - column 6, line 11}.

In re claim 7, Hatanaka shows wherein the disposing step is performed so that the terminal of the second integrated circuit is not covered by the first integrated circuit {column 3, line 5 - column 6, line 11}.

In re claim 16, Hatanaka includes providing the energy pulse in the form of a current which is applied to the electrically conductive connection {column 3, line 5 - column 6, line 11}.

In re claim 17, Hatanaka includes providing the energy pulse in the form of a laser beam which is applied to the electrically conductive connection {column 3, line 5 - column 6, line 11}.

In re claim 18, Hatanaka includes performing the severing step before packaging the first and second integrated circuits {column 3, line 5 - column 6, line 11}.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hatanaka in view of Kuriyama.

In re claim 5, Hatanaka substantially discloses the invention as claimed but fails to show disposing the first and second integrated circuits in a package having terminal pins so that the signal terminal of the first integrated circuit is not accessible from outside of the package; and connecting the terminal of the first integrated circuit and the terminal of the second integrated circuit to a respective terminal pin of the package.

Kuriyama shows disposing first and second integrated circuits, substantially equivalent in structure and effect to the first and second integrated circuits of Hatanaka, in a package having terminal pins (2/4/5) so that the signal terminal of the first integrated circuit is not accessible form outside of the package; and connecting the terminal of the first integrated circuit and the terminal of

the second integrated circuit to a respective terminal pin (5/4) of the package {column 3, lines 4-54}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to dispose the first and second integrated circuits of Hatanaka in a package such as that found in Kuriyama (i.e., a package having terminal pins) so that the signal terminal of the first integrated circuit is not accessible from outside of the package and so that the terminal of the first and second integrated circuits are connected to respective terminal pins of the package since the package of Kuriyama would enable the integrated circuit device of Hatanaka to be protected and selectively accessible to other integrated circuit components that would enable the functionality of the device of Hatanaka to be realized.

In re claim 6, Hatanaka substantially discloses the invention as claimed but fails to show wherein the severing step if performed after the step of connecting the respective terminals to the respective terminal pins.

Kuriyama shows wherein a severing step is performed after the step of connecting the respective terminals to the respective terminal pins {column 3, lines 4-54}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the severing step of Hatanaka in view of Kuriyama after the step of connecting the respective terminals to the respective terminal pins since as in Kuriyama since severing electrical connections by blowing fuses after semiconductor devices have been packaged is well known in the art the selection of the placement of a fuse blowing step within a fabrication sequence on the basis of its suitability involves only routine skill in the art.

6. Claims 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hatanaka in view of Kuriyama in view of Bozso.

In re claim 8, Hatanaka shows in Figures 1A-1B, 2A-2B, 3, 4, and 5A-5I a method for producing an electrical connection between integrated circuits which includes providing a first integrated circuit having a surface; disposing first and second terminal pads (10 and 3, respectively); forming an electrically conductive connection (11) between the first and second terminal pads of the first integrated circuit; providing a second integrated circuit having a surface; disposing first and second terminal pads (10 and portion of gate electrode 21 or 22 which electrically contacts first conductive line 6, respectively) on the surface of the second integrated circuit; providing a protective structure (23/24) that becomes conductive to dissipate electrostatic discharges; electrically coupling at least the first terminal pad of the second integrated circuit to the protective structure; disposing the surfaces of the first and second integrated circuits latitudinally adjacent one another so that the first and second terminal pads of the second integrated circuit are not covered by the first integrated circuit; electrically joining at least one of the first and second terminal pads of the first integrated circuit to one of the first and second terminal pads of the second integrated circuit; and severing the electrically conductive connection using an energy pulse. Hatanaka also shows wherein the first and second integrated circuits are formed on a single substrate {column 3, line 5 - column 6, line 11}.

Hatanaka does not show disposing the surfaces of the first and second integrated circuits longitudinally adjacent one another so that the first and second terminal pads of the second integrated circuit are not covered by the first integrated circuit.

Kuriyama shows in Figures 1, 2, and 9 a method for producing an electrical connection between integrated circuits, providing a first integrated circuit (7) having a surface; disposing first and second terminal pads (11 and 12) on the surface of the first integrated circuit; forming an electrically conductive connection (10c) between the first and second terminal pads of the first integrated circuit; providing a second integrated circuit (3) having a surface; disposing first and

second terminal pads (3b and 3c) on the surface of the second integrated circuit; electrically coupling at least the first terminal pad of the second integrated circuit to a protective structure for protecting against electrostatic discharges; disposing the surfaces of the first and second integrated circuits adjacent one another latitudinally; electrically joining at least one of the first and second terminal pads of the first integrated circuit to one of the first and second terminal pads of the second integrated circuit; and severing the electrically conductive connection using an energy pulse. Kuriyama also shows wherein the first and second integrated circuits may be formed on a single substrate or on separate substrates, electrically connected to each other in both cases. { column 3, line 4 – column 4, line 10}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the first and second integrated circuits of Hatanaka on separate substrates since, as evidenced by Kuriyama, the provision of individual circuits included in an integrated circuit package on a electrically connected on a single substrate or electrically connected on separate substrates is well known in the art and the separation of a formerly integral structure into pieces of that formerly integral structure involves only routine skill in the art when the effects of the pieces is substantially the same as the effects of the formerly integral structure.

Hatanaka in view of Kuriyama still does not show the surfaces of the first and second integrated circuits longitudinally adjacent one another so that the first and second terminal pads of the second integrated circuit are not covered by the first integrated circuit.

Bozso shows in Figure 7 that two integrated circuits may be bonded together by disposing surfaces of the integrated circuits longitudinally adjacent one another so that terminal pads of one of the integrated circuits are not covered by the other integrated circuit {column 5, lines 36-39}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to dispose the surfaces of the first and second integrated circuits of Hatanaka in view of Kuriyama longitudinally adjacent one another so that the first and second terminal pads of the second integrated circuit are not covered by the first integrated circuit as in Bozso since, as evidenced by Bozso, it is well known within the packaging art to place two integrated circuits together such that their surfaces are longitudinally adjacent one another and the packaging arrangement of Bozso would provide a compact package with which to use. Furthermore, the specification contains no disclosure of either the critical nature of the claimed packaging arrangement or any unexpected results arising therefrom. Where patentability is said to be based on a particular packaging arrangement or upon another variable recited in a claim, the applicant must show that the claimed packing arrangements are critical or yield unexpected results over the prior art.

In re claim 9, Hatanaka shows wherein the electrically joining step is performed using an electrically conductive solderable material {column 3, line 5 - column 6, line 11}.

In re claim 10, Hatanaka shows wherein the electrically joining step is performed using a conductive adhesive material {column 3, line 5 - column 6, line 11}.

In re claim 11, Hatanaka includes electrically joining the other one of the first and second terminal pads of the first integrated circuit to the other one of the first and second terminal pads of the second integrated circuit {column 3, line 5 - column 6, line 11}.

Response to Arguments

7. Applicant's arguments with respect to claims 1-11 and 16-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Paper related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication of earlier communication from the examiner should be directed to **Kurt Eaton** at **(703) 305-0383** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via kurt.eaton@uspto.gov.

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